Issue 7, 1984 : Computer 4

commodore TECHTOPICS

Model: C16, PLUS 4

LINE DEFINITIONS

A0 to A15	Address Bit 0 to 15
AEC	Address Enable Control
ATN	Attention
BA	Bus Available
BRESET	Buffered System Reset
C1 HIGH, C1 LOW	External Cartridge Chip Select
C2 HIGH, C2 LOW	"
CAS	Dynamic RAM Column Address Strobe
CLK IN	Master Clock (Single Phase, 14.31818 MHz)
COLOR	Chroma Output
COMP	Composite Chroma and Luma
CE	Chip Enable
CS	Chip Select
CS0	Low ROM Chip Select
CS1	High ROM Chip Select
CST MTR	Cassette Motor Control
CST RD	Cassette Read
CST SENSE	Cassette Sensor
CST WRT	Cassette Write
CTS	Clear To Send
DB0 to DB7	Data Bit 0 to 7
DCD	Data Carrier Detect
DRAM	Dynamic RAM
DRAM ADD	Dynamic RAM Address
DSR	Data Set Ready
DTR	Data Terminal Ready
EXT AUDIO	External Audio Input
GATE IN	R/W GATE
IRQ	Interupt Request
K0 to K7	Keyboard Latch 0 to 7
KERN	Kernal ROM Control Line
LUM	Composite Sync and Luminence
MUX	Address Multiplex Control
P0 to P7	Port Bit 0 to 7
RAS	Dynamic RAM Row Address Strobe
RESET	System Reset
RxC	Receive Clock
RxD	Receive Data
R/W	Read/Write Line
RTS	Request To Send
SND	Sound Line
TED	Text Display
TxD	Transmit Data
ϕ 0	System Clock (Varies between 1 and 2 MHz)
ϕ 2	Artificial ϕ 2, Address Valid Rising Edge, Data Valid Falling Edge